CLAIMS

1-62. (Canceled)

63. (Currently amended) ~~A data processing apparatus as set forth in claim 60~~ A data processing apparatus comprising:

a central processing unit configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal, a first signal and a second signal being input to said central processing unit as said interrupt request signal,

wherein said central processing unit executes a program code, said program code being stored in memory at a program address,

wherein said memory is random access memory,

wherein a counter register is located within said random access memory, said counter register being incremented when said program address coincides with ~~said~~ a first bug address or ~~said~~ a second bug address.

64. (Currently amended) ~~A data processing apparatus as set forth in claim 57~~ A data processing apparatus comprising:

a central processing unit configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal, a first signal and a second signal being input to said central processing unit as said interrupt request signal,

wherein said central processing unit executes a program code, said program code being stored in memory at a program address,

wherein said first signal indicates when said program address and a first bug address coincide, said second signal indicating when said program address and a second bug address coincide.

65. (Previously presented) A data processing apparatus as set forth in claim 64, wherein a first coincidence detecting circuit compares said program address with said first bug address, said first coincidence detecting circuit outputting said first signal when said program address and said first bug address coincide.

66. (Previously presented) A data processing apparatus as set forth in claim 65, wherein a second coincidence detecting circuit compares said program address with said second bug address, said second coincidence detecting circuit outputting said second signal when said program address and said second bug address coincide.

67. (Previously presented) A data processing apparatus as set forth in claim 66, wherein a number of times said first and second bug addresses coincide with said program address is counted, a value representing said number of times.

68. (Previously presented) A data processing apparatus as set forth in claim 67, wherein said first bug address indicates a starting address for a first buggy part of a program or data, said second bug address indicating a starting address for a second buggy part of said program or data.

69. (Previously presented) A data processing apparatus as set forth in claim 68, wherein said first buggy part or said second buggy part is selected for correction, said central processing unit using said value to select said first buggy part or said second buggy part.

70. (New) A data processing apparatus as set forth in claim 64, wherein said first and second signals are input to an AND gate, an output from said AND gate being input to said central processing unit as said interrupt request signal.

71. (New) A data processing apparatus as set forth in claim 64, wherein said first and second signals are input to said central processing unit as a single signal.

72. (New) A data processing apparatus as set forth in claim 64, wherein said first and second signals are input to said central processing unit as two different signals.

73. (New) A data processing apparatus as set forth in claim 64, wherein said program address is a count of a program counter.

74. (New) A data processing apparatus as set forth in claim 64, wherein said memory is read only memory.

75. (New) A data processing apparatus as set forth in claim 64, wherein said memory is random access memory.

76. (New) A data processing apparatus as set forth in claim 75, wherein said interrupt processing routine is stored in said random access memory.

77. (New) A data processing apparatus as set forth in claim 75, wherein an abort vector is stored in said random access memory, said abort vector designating a start address of said interrupt processing routine.

78. (New) A data processing apparatus as set forth in claim 75, wherein a counter register is located within said random access memory, said counter register being incremented when said program address coincides with said first bug address or said second bug address.